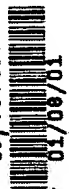


10903 U.S. PTO
09/757404



Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

JCT
60

O.I.P.E. 12W SCANNED Hkm Q.A.	PATENT DATE
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APPLICATION NO. 09/757404	CONT/PRIOR	CLASS 703	SUBCLASS 14	ART UNIT 2123	EXAMINER Broda HOGAN
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APPLICANTS

Steven Guccione
Scott McMillan
Brandon Blodget

TITLE

Method and system for device-level simulation of a circuit design for a programmable logic device

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							

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	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED _____	
	_____ (Primary Examiner) _____ (Date)			ISSUE FEE Amount Due Date Paid	
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